REMARKS

Reconsideration is requested in view of the above amendments and the following remarks. Claim 1 has been revised to include the feature of claim 4. Claim 5 has been revised to depend from claim 1. Claim 4 has been canceled accordingly. New claim 10 has been added. Support for claim 10 can be found at, e.g., paragraph [0012] of the specification, among other places. Claims 1, 3 and 5-10 are pending in the application.

Claims 1 and 4-9 are rejected under 35 USC 103(a) as being unpatentable over Iechi et al. (US Publication No. 2003/0213952) in view of Arai et al. (JP 07-297406). Applicants respectfully traverse this rejection. Claim 1 has been revised to include the feature of claim 4. Claim 5 has been revised to depend from claim 1. Claim 4 has been canceled accordingly.

Claim 1 requires a thin film transistor unit and a display element unit that are laminated on a substrate in this order. That is, the thin film transistor unit is positioned between the display element unit and the substrate. As a result, the thin film transistor is covered by the display element unit such that the distance that gas and moisture have to travel to reach an active layer of the transistor unit from outside has advantageously been increased, without increasing the number of constituent members of the display apparatus. This effectively suppresses the permeation of gas and moisture from the atmosphere into the thin film transistor unit and avoids deterioration of the physical property of the thin film transistor unit, thus helping to extend the life of the display apparatus (see e.g., page 3, lines 23-27 and page 10, lines 13-20 of the specification, among other places).

Iechi et al. fail to teach or suggest a thin film transistor unit and a display element unit that are laminated on a substrate in this order, as required by claim 1. Instead, as shown in Fig. 2, Iechi et al. discuss a drain electrode 12, a semiconductor layer 13 and a source electrode 15 formed one by one in this sequence on the upper surface of a substrate 11, where the semiconductor layer 13 is made from an electric field luminescent (EL) semiconductor material (see Iechi et al., paragraph [0036]). Iechi et al. are completely silent as to the order of how the thin film transistor unit, the display element unit and a substrate are positioned, much less any reason to expect the advantages that are

enjoyed by the present invention, e.g., suppressing the permeation of gas and moisture from the atmosphere into the thin film transistor unit, could be achieved.

Moreover, Iechi et al. merely discuss a semiconductor layer 13 that is made from an EL semiconductor material, but fail to teach or suggest that a thin film transistor unit and a display element unit are laminated on a substrate in this order, as required by claim 1. The semiconductor layer 13 referred in Fig. 2 of Iechi et al. includes only one structural member, rather than two structural members, for example, a thin film transistor unit and a display element unit, as recited in claim 1. There is no basis for arbitrarily dividing the Iechi et al. semiconductor layer 12 into different features, as the rejection requires to meet claim 1.

Arai et al. do not remedy the deficiencies of Iechi et al. In addition, it would not have been obvious to combine the vertical TFT device in Arai et al. with Iechi et al. in the manner suggested by the rejection. The mere fact that references can be combined does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination (see MPEP §2143.01 III). Nothing in the present record suggests that the vertical TFT device discussed in Arai et al. including drain electrodes 11 and 12 that have larger areas than that of the source electrode 14 be used for the Iechi et al. transistor. Nor does the present record provide any reason to use a drain electrode that has an area larger than that of a source electrode to, e.g., produce large current, in the transistor 20 of Iechi et al.

For at least these reasons, claim 1 is patentable over Iechi et al. in view of Arai et al. Claims 4-9 depend from claim 1 and are patentable along with claim 1 and need not be separately distinguished at this time. Applicants are not conceding the relevance of the rejection to the remaining features of the rejected claims.

Claims 1 and 3 are rejected under 35 USC 103(a) as being unpatentable over Iechi et al. in view of Morita et al. (JP 2003-084686). Applicants respectfully traverse this rejection. As discussed above, Iechi et al. fail to teach or suggest a thin film transistor unit and a display element unit that are laminated on a substrate in this order, as required by claim 1. Morita et al. do not remedy the deficiencies of Iechi et al. For at least these

reasons, claim 1 is patentable over Iechi et al. in view of Arai et al. Claim 3 depends from claim 1 and is patentable along with claim 1 and need not be separately distinguished at this time. Applicants are not conceding the relevance of the rejection to the remaining features of the rejected claims.

In view of the above, favorable reconsideration in the form of a notice of allowance is respectfully requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612) 455-3804.

Respectfully submitted,

HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. Box 2902-0902
Minneapolis, MN 55402-0902
(612) 455-3800

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By: _____
Douglas P. Mueller
Reg. No. 30,300

DPM/cy